

PATENT
Attorney Docket N° 03-0805

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Sean C. Erickson, et al.
Serial : 10/627,289
Filed : July 25, 2003
Group Art Unit : 2814
Examiner : Trinh, Hoa B.
For : LOW GATE RESISTANCE LAYOUT PROCEDURE FOR RF
TRANSISTOR DEVICES

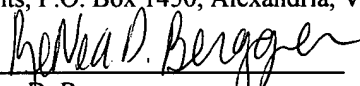
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR A ONE-MONTH EXTENSION OF TIME
PURSUANT TO 37 C.F.R. §1.136(a)

CERTIFICATE OF MAILING 37 C.F.R. § 1.8

MAILING

☒ deposited with the United States Postal Service
with sufficient postage as first class mail in an
envelope addressed to the Commissioner for
Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


ReNea D. Berggren

FACSIMILE

☐ transmitted by facsimile to the Patent and
Trademark Office.

DATED: April 1, 2005

Applicant hereby requests a one month extension of time for response to the *Final Office Action* herein dated December 28, 2004. The grant of this *Petition* will extend the time for response from March 28, 2005 to April 28, 2005.

Please charge the extension fee of **\$120.00** to Deposit Account N° 12-2252. Please charge any underpayments related to this *Petition* or credit any excess to Deposit Account N° 12-2252. A duplicate copy of this *Petition* is enclosed for accounting purposes only.

04/05/2005 AWONDAF1 00000065 122252 10627289

02 FC:1251 120.00 DA

Please address all correspondence to:

CUSTOMER NO. 24319

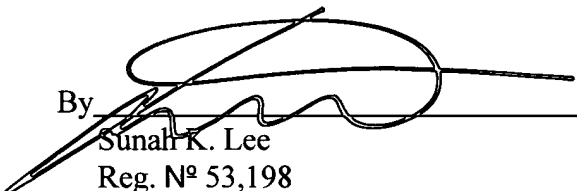
PETER SCOTT
LEGAL DEPARTMENT - IP
LSI LOGIC CORPORATION
M/S D-106
1621 BARBER LANE
MILPITAS, CA 95035

DATED: April 1, 2005.

Respectfully submitted,

Sean C. Erickson, et al.,
LSI Logic Corporation,

By



Sunah K. Lee
Reg. N° 53,198

SEAN PATRICK SUITER
SUITER • WEST PC LLO
14301 FNB Parkway, Suite 220
Omaha, NE 68154-5299
(402) 496-0300 (Telephone)
(402) 496-0333 (Telecopier)